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PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application No. :	10/605,408	Confirmation No. 2407
Applicant :	Kern Rim	
Filed:	September 29, 2003	
TC/Art Unit:	2813	
Examiner :	James M. Mitchell	
Docket No. :	YOR920000707US2	
Customer No. :	27127	

Commissioner for Patents  
P.O. Box 1450  
Alexandria VA 22313-1450

**DECLARATION UNDER 37 CFR §1.131**

I, Kern Rim, depose and say that:

- (1) I am the sole inventor of the subject matter covered by each of the claims pending in the above-identified U.S. patent application (the "Application").
- (2) I am currently employed with International Business Machines Corp. (IBM), the assignee of the Application.
- (3) Prior to February 7, 2002, I conceived and completed, in this country, my disclosed and claimed invention for a method of forming a strained silicon-on-insulator (SSOI) structure involving the steps of: forming a silicon layer on a strain-inducing layer with a different lattice constant than

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silicon so that the silicon layer is strained; bonding the resulting multilayer structure to a substrate so that an insulating layer is between the strained silicon layer and the substrate; and then removing the strain-inducing layer to yield a strained silicon-on-insulator structure comprising the substrate, the insulating layer on the substrate, and the strained silicon layer on the insulating layer. Completion of this method is evidenced attached hereto as Exhibits A through G, each of which are documents in existence prior to February 7, 2002.

- (4) Exhibit A is a split table detailing eight "wafer types" to be prepared according to the method recited in claims of the Application.
- (5) Exhibit B is an email in which I requested 20% SiGe wafers identified in the table of Exhibit A.
- (6) Exhibit C is an email confirming receipt of the wafers requested in Exhibit B and discussing an experiment underway on the wafers. At this point the success of the process was uncertain, as evident from this email.
- (7) Exhibit D is an email reporting progress in the experiment and requesting assistance in removing the strain-inducing SiGe layer from the experimental wafers.

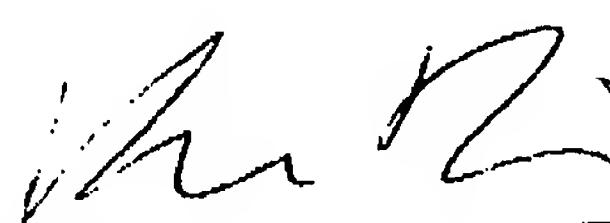
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(8) Exhibit E is an email which expresses anticipated good results when the experiment is completed within a period prior to February 7, 2002.

(9) Exhibit F is an email that discusses carrying out the final step of etching to remove the SiGe layer of the SSOI wafers already processed in the experiment. This final step was successfully completed prior to February 7, 2002. In particular, I recall that Kevin Chan (also an employee of IBM) and I completed experiments prior to 2002, during which we removed the SiGe layer of the SSOI wafers by CMP and etch and confirmed (I believe by deep UV Raman spectroscopy) that the strain was retained in the silicon layers after removal of the SiGe layers. Furthermore, by the time I submitted my invention disclosure to the IBM Intellectual Property Law Department in 2000, I had concluded that the bond strength at the Si-SiO<sub>2</sub> interface would be strong enough to retain the strain in the Si layer based on my research of published bonding energy information. Therefore, even before I confirmed the strain retention through actual testing (as discussed above), I had high confidence that my invention of a silicon layer with strain induced by a SiGe layer and then bonded to an oxide layer would remain strained after removing the SiGe layer.

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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.



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Kern Rim

Exhibit A

A SSST1	B	C	D	E	F
Wf#	Wafer ID	Wafer Type	Wafer Note	Description	Description
1	MS18E9P	20%	20SS06 350A	SSOI	
2	ME18CNF	20%	20SS06 350A	SSOI	
3	ME18NPF	15%	15SS02 350A	SSOI	
4	ME18WBF	15%	15SS02 350A	SSOI	
5	ME18BLF	A 20% SiGe + 500A Si	DSC002	Control thin SOI	
6	MS188VP	A 20% SiGe + 500A Si	DSC002	Control thin SOI	
7	M2187RF	A 20% SiGe + 500A Si	DSC002	Control thin SOI	
8	M7187RF	A 20% SiGe + 500A Si	DSC002	Control thin SOI	

Experiment Split Table from  
 [REDACTED]  
 File name: SSOI.123

## Exhibit B

  
Ken Rim/Matson/IBM

To: Jack O Chu  
cc  
bcc

Subject: wafers

Jack,

I would like to release Center 1 device lot next week. How is the wafer situation these days? I'd need 5 15% and 5 20% wafers.

Other wafer needs that are imminent:

SSOI experiment: 4 with ~500 Å pseudomorphic SiGe 20%  
2-3 SiGe buffer wafers (Si cap does not matter) for CMP practice (don't have to  
be device grade)

Ron's silicide experiment.

I'll give you a call when I get back tomorrow. Thanks!

Ken

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Ken Rim  
IBM T. J. Watson Research Center  
P. O. Box 218 / Route 134  
Yorktown Heights, NY 10598  
Phone: 914-945-2846  
E-mail: [rim@us.ibm.com](mailto:rim@us.ibm.com)

## **Exhibit C**

Ken Rim/WatsonIBM  
To: Erin C Jones/WatsonIBM@IBMWUS  
cc: Meekai Leong/FishkillIBM@IBMWUS  
bcc:

To [Erin.C.Jones@IBMUS](mailto:Erin.C.Jones@IBMUS)  
cc [Mekai.Leong/FishkillIBM@IBMUS](mailto:Mekai.Leong/FishkillIBM@IBMUS)  
bcc

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Remember that crazy idea I talked to you about back in fall? Transferring strained Si right on insulator?

I finally got a few wafers from Jack and gave them to Leathen. (We had the supertek run sheet written a while ago.) The goal of this experiment is simply to check if the transferred layer can retain any of the strain. If any of the strain is indeed retained, we will want to do some annealing experiments, and I am hoping your group (Kevin, new hire, etc.) and Jack can help with taking the idea further. It's essentially very similar to what is known as "Ultra-Cut", and should be interesting just a way to create a thin, uniform SOI even if it is not strained.

I think it is a risky experiment in terms of rate of success, but if it works, I think this could be something we can consider for beyond 11S.

Just thought I would let you know in case you have any concerns or objections. Right now, I wanted to keep it as a very low key low profile experiment, mostly because it might turn out to be a bad idea.

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IBM T. J. Watson Research Center  
P. O. Box 218, Route 134  
Yorktown Heights, NY 10598  
Phone: 914-945-2946  
E-mail: [rim@us.ibm.com](mailto:rim@us.ibm.com)

## Exhibit D

Jack,

Leahen finished bonding, grinding back, and CMP on the strained Si-directly-on-insulator. He has 6 (I think) wafers. A couple of them are control wafers with Si/pseudomorphic SiGe stacks.

The next steps were going to be thickness measurement by nanospec, litho patterning to put some patterns for easy step height measurement, and careful selective etch of SiGe. Since I've been busy, I've been just waiting for the right moment to do this.

When you mentioned the SSOI at today's meeting, I just remembered. Since you have some experience with HHA etch, and since you may have some time now while your reactor is down, if you want to join this experiment, maybe you can help with the etch back? I was going to first do some etch rate test on blanket SiGe wafers, and then break up one of the wafers to try the etch back on pieces.

Let me know if you are interested.

Thanks.

Ken

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Ken Rim  
IBM T. J. Watson Research Center  
P. O. Box 218 / Route 134  
Yorktown Heights, NY 10598  
Phone: 914-945-2946  
E-mail: rim@us.ibm.com

---

To Jack O Chu@Watson@IBMUS  
cc Leahen Shu@Watson@IBMUS  
bcc  
Subject SSOI experiment

## Exhibit E

Jack O ChuWatson/IBM  
[REDACTED]

To Ken RimWatson/IBM@IBMUS, Erin C  
JonesWatson/IBM@IBMUS, Meikei  
Leong/FishkillIBM@IBMUS, Kevin K  
ChanWatson/IBM@IBMUS, Suri  
HegdeWatson/IBM@IBMUS, Leathen  
ShiWatson/IBM@IBMUS, Alfred  
GrillWatson/IBM@IBMUS, H-S Philip  
WongWatson/IBM@IBMUS

bcc

Subject 'IBM Confidential: SSOI and SGCI'

- Ken,

I've already started a couple of runs with Leathen for making t-SGOI & SSOI and hopefully in the next month or so, I'll have some "good" results.

-- Jack

Dr. Jack O. Chu  
Electronic Materials & Structures Group  
IBM T.J. Watson Research Center

Internet: chuj@us.ibm.com  
Notes: Jack O. ChuWatson/IBM@IBMUS  
Phone: (914) 945-2709, Fax: 945-4581

----- Forwarded by Jack O ChuWatson/IBM on [REDACTED] 12:16 PM -----

Ken Rim  
[REDACTED]

To: Erin C JonesWatson/IBM@IBMUS, Kevin K ChanWatson/IBM@IBMUS, Suri  
HegdeWatson/IBM@IBMUS, Leathen ShiWatson/IBM@IBMUS, Jack O ChuWatson/IBM@IBMUS  
cc: Meikei Leong/FishkillIBM@IBMUS  
From: Ken RimWatson/IBM@IBMUS  
Subject: 'IBM Confidential: SSOI and SGCI'

## Exhibit F

Ken RimWatson/IBM  
[REDACTED]

To Jack O ChuWatson/IBM@IBMUS

cc Alfred GrillWatson/IBM@IBMUS, Erin C

JonesWatson/IBM@IBMUS, Kevin K

ChauWatson/IBM@IBMUS, Leathen

ShiWatson/IBM@IBMUS, Meikei

LeongFFishkillIBM@IBMUS, Suri

HegdeWatson/IBM@IBMUS

bcc

Subject Re: "IBM Confidential: SSOI and SGO" [REDACTED]

Jack,

How far are you along with the process? Leathen bonded a few SSOI wafers(wafers you grew) for me (just SSOI, not SGO) back last winter, and they have been just waiting for the HHA etching experiments. So they are already etched back down to the SiGe layer, and I just never had time to do the next steps- iterations to etch SiGe and stop on Si. I was going to ask Suri to help us drive this experiment and start a new batch with a couple of other ideas. Can we work with you, especially on these few wafers that are all ready for the last step, to get the HHA etch to work?

Ken

---

Ken Rim  
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P.O. Box 1450  
Alexandria VA 22313-1450

DECLARATION UNDER 37 CFR §1.131

I, Kevin C. Chan, depose and say that:

- (1) I am currently employed with International Business Machines Corp. (IBM), the assignee of the above-identified U.S. patent application (the "Application"), as a researcher at the IBM T. J. Watson Research Center.
- (2) I am very familiar with the method described in the original and pending claims of the Application.
- (3) I assisted Kern (Ken) Rim, the inventor and applicant of the Application, in completing the invention described in the Application by performing and completing experiments on behalf of Mr. Rim.

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(4) As evidenced by the attached pages of my experiment notebooks, the SiGe material and method described and claimed in the Application were successfully developed and completed prior to February 7, 2002. Included in the attached pages, under the title "RTCVD SiGe 25% (repeated) with 200A strained-Si," are the parameters employed in the successful method, including process flow rate, pressure, temperature, and wafer ID.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

  
\_\_\_\_\_  
Kevin C. Chan

12/13/06

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Attachment Contents:

- Page 1 Title and number of IBM official research laboratory notebook, which is systematically dated from 1986 to present. This particular notebook #13 was started prior to the year 2001, and contains the following Pages 2 through 5.
- Page 2 Notes from discussion with Ken Rim. Experiment and structure set up.
- Page 3 Experimental results of a film stack which created strained silicon from SiGe.
- Page 4 Email in which Ken Rim requested wafers for transistor fabrication.
- Page 5 Material results verification for strained silicon.

Attachment to Declaration of Kevin C. Chan  
Page 1

LABORATORY NOTEBOOK

Assigned to:	Kevin C. Chan
Date:	[Redacted]
Notes:	[Redacted]
Comments:	[Redacted]
Page:	[Redacted]

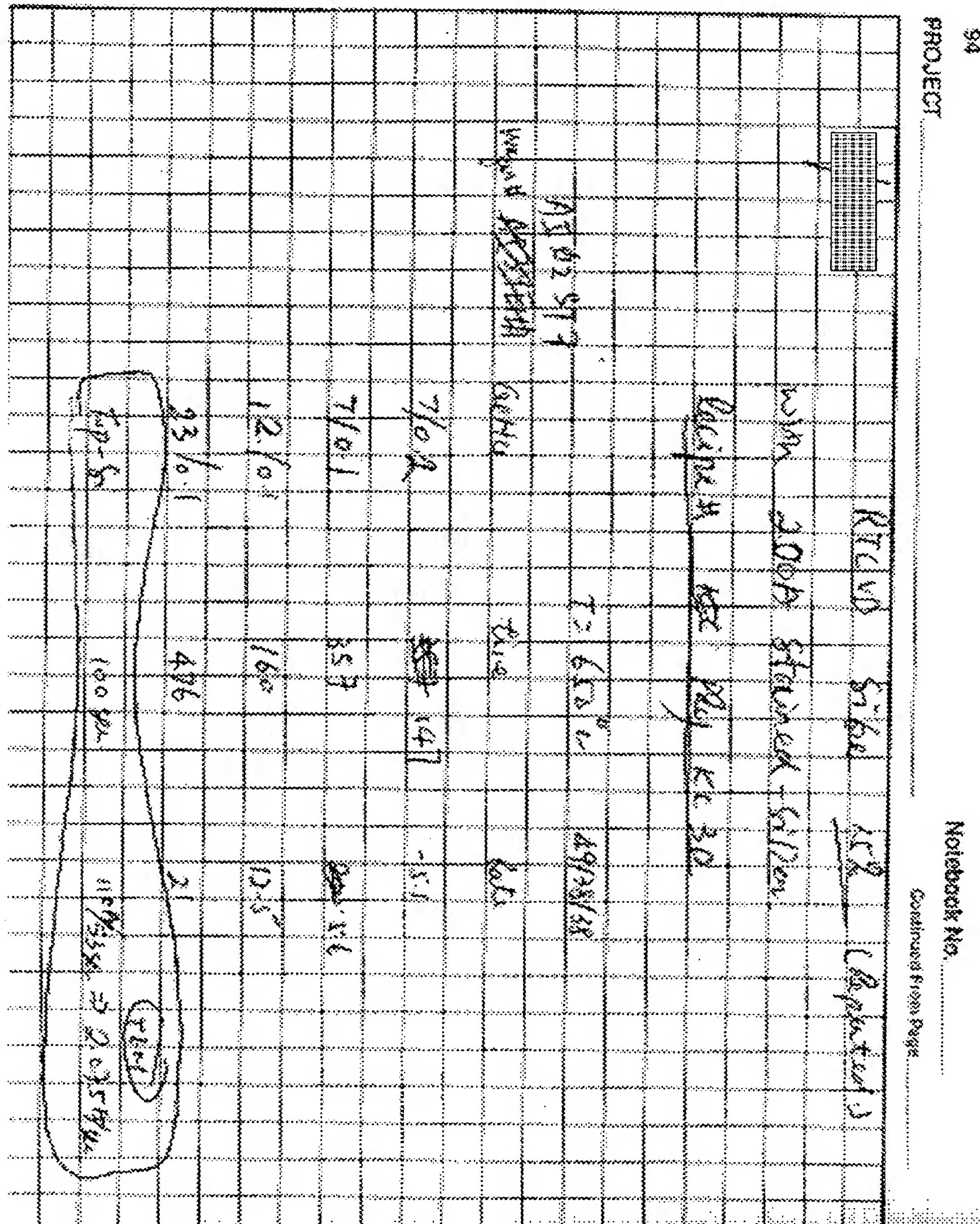
Attachment to Declaration of Kevin C. Chan  
Page 2

Attachment to Declaration of Kevin C. Chan  
Page 3

A high-contrast, black and white image showing a grid pattern, likely a window or screen. The grid consists of thin, light-colored lines forming a regular grid of squares. Numerous small, dark, irregular shapes are scattered across the surface, varying in size and density. These shapes resemble dust particles, scratches, or noise. The overall texture is grainy and lacks fine detail due to the high contrast.

Attachment to Declaration of Kevin C. Chan  
Page 4

Attachment to Declaration of Kevin C. Chan  
Page 5



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